Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of the Claims:

1. (Currently Amended) A nonvolatile memory comprising:

a first terminal;

a second terminal;

a controller; and

nonvolatile memory cells,

wherein said first terminal is for receiving pulses of a first signal,

wherein said second terminal is for receiving data, and

wherein said controller is adapted to control (i) ~~the~~ a receiving of address information, (ii) ~~the~~ a receiving of a first data via said second terminal in response to the pulses of said first signal received from said first terminal, and (iii) ~~the~~ after said receiving of data, a performing of a data writing to write said first data to ones of said nonvolatile memory cells corresponding to said address information without receiving pulses of said first signal via said first terminal until completion of said performing of data writing.

2. (Currently Amended) A nonvolatile memory according to claim 1,

wherein said nonvolatile memory controls ~~the~~ a performing of a verify operation for checking whether said data writing is completed or not, after performing said data writing without receiving pulses of said first signal via said first terminal.

3. (Currently Amended) A nonvolatile memory according to claim 2, further comprising a power generating circuit,

wherein said power generating circuit is configured to generate a program voltage for use in ~~writing~~ said data writing, and

wherein said controller enables said power generating circuit to generate said program voltage during said performing of said data writing.

4. (Currently Amended) A nonvolatile memory according to claim 3,

wherein ~~said controller is capable of receiving a 512 Byte length unit as~~ said first data is 512 bytes in length, and

wherein said ones of nonvolatile memory cells corresponding to said address information are capable of storing data of more than 512 ~~Bytes~~ bytes in length.

5. (Currently Amended) A nonvolatile memory comprising:

a first terminal;

a second terminal;

a controller; and

a plurality of nonvolatile memory arrays,

wherein said first terminal is capable of receiving pulses of a first signal,

wherein said second terminal is capable of receiving data,

wherein each of said plurality of nonvolatile memory arrays includes a plurality of nonvolatile memory cells,

wherein said controller is adapted to control (i) ~~the~~ a receiving of a first address information, (ii) ~~the~~ a receiving of first data via said second terminal in response to ~~the~~ said pulses of said first signal, ~~and~~ (iii) ~~the~~ after said receiving of said first data, a selecting of a first one of said plurality of nonvolatile memory arrays, corresponding to said first address information, and then (iv) ~~the~~ a writing of said first data ~~therein~~ to said first one of said plurality of nonvolatile memory arrays without receiving said pulses of said first signal during a period of said writing of said first data, and

wherein said first one of said plurality of nonvolatile memory arrays is capable of performing writing of said first data to ones of said plurality of nonvolatile memory cells therein corresponding to said first address information ~~without receiving pulses of said first signal~~.

6. (Currently Amended) A nonvolatile memory according to claim 5,

wherein said controller further controls ~~(iv) the~~ (v) a receiving of a second address information, ~~(v) the~~ (vi) a receiving of a second data via said second terminal in response to the pulses of said first signal, ~~and (iv) the~~ (vii) after said receiving of said second data, a selecting of a second one of said plurality of nonvolatile memory arrays, corresponding to said second address information, and then (viii) ~~the~~ a writing of said second data ~~therein~~ to said second one of said plurality of nonvolatile memory arrays without receiving said pulses of said first signal during a period of said writing of said second data, and

wherein said second one of said plurality of nonvolatile memory arrays is capable of performing writing of said second data to ones of said

nonvolatile memory cells therein corresponding to said second address information ~~without receiving pulses of said first signal~~.

7. (Currently Amended) A nonvolatile memory according to claim 6,

wherein each of said plurality of nonvolatile memory arrays performs a verify operation for checking whether or not a data writing is completed therein, in the performance of a writing operation.

8. (Currently Amended) A nonvolatile memory according to claim 7,

wherein each of said plurality of nonvolatile memory arrays performs an erase operation for erasing data stored in ones of said plurality of nonvolatile memory cells, and

wherein said second one of said plurality of nonvolatile memory arrays is capable of performing said erase operation for erasing data stored in ones of nonvolatile memory cells therein corresponding to said second address information ~~in a~~ during said writing ~~operation~~ of said first data in said first one of said plurality of nonvolatile memory arrays.

9. (Currently Amended) A nonvolatile memory according to claim 8,

wherein each of said first data and said second data is 512 ~~Bytes~~ bytes in length, ~~and~~

wherein said ones of said nonvolatile memory cells in said first one of nonvolatile memory arrays are capable of being written with more than a 512 ~~Byte~~ byte length data, and

wherein said ones of said nonvolatile memory cells in said second one of nonvolatile memory arrays are capable of being written with more than a 512 ~~Byte~~ byte length data.

10. (New) A nonvolatile memory comprising:

a data terminal;

a clock terminal;

a controller; and

a first nonvolatile memory array,

wherein said controller is adapted to control (i) a receiving of a first data and (ii) a writing of said first data to said first nonvolatile memory array,

wherein during said receiving of said first data, said controller controls a latching of said first data, inputted via said data terminal, in response to pulses of a first signal received from said clock terminal, and

wherein during said writing of said first data, said controller controls a storing of said first data into said first nonvolatile memory array without receiving said pulses of said first signal.

11. (New) A nonvolatile memory according to claim 10,

wherein said first data is 512 bytes in length, and

wherein said nonvolatile memory is capable of storing data having more than 512 bytes in length, at a time.

12. (New) A nonvolatile memory according to claim 11,

wherein said controller is structured on a first semiconductor chip, and

wherein said first nonvolatile memory array is structured on a second semiconductor chip, different from said first semiconductor chip.

13. (New) A nonvolatile memory according to claim 12, further comprising a second nonvolatile memory array,

wherein said second nonvolatile memory array is structured on a third semiconductor chip, different from said first and second semiconductor chips,

wherein said controller is adapted to control (iii) a receiving of a second data and (iv) a writing of said second data to said second nonvolatile memory array,

wherein during said receiving of said second data, said controller controls a latching of said second data, inputted via said data terminal, in response to said pulses of said first signal, and

wherein during said writing of said second data, said controller controls a storing of said second data into said second nonvolatile memory array without receiving said pulses of said first signal.

14. (New) A nonvolatile memory according to claim 13,

wherein each of said first data and said second data is 512 bytes in length, and

wherein each of said first nonvolatile memory array and said second nonvolatile memory array is capable of storing data having more than 512 bytes in length.